A GPS FAST ACQUISITION RECEIVER

by

Eric D. Holm

Edwin E. Westerfield

The Johns Hopkins University
Applied Physics Laboratory

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Abstract

The Air Force's Global Positioning System (GPS) can be used to determine the position of equipment under test on various military test ranges. Many range uses require that position information be available immediately upon launch. APL is developing a receiver capable of acquiring GPS satellite signals within a few tenths of a second. The receiver concept is based on the same tracking algorithm used successfully for 5 years in other GPS application programs developed at the Applied Physics Laboratory. The receiver however, will be enhanced to gain the capability of searching 1023 code phases in parallel. The techniques used within the receiver to implement the parallel operation are described.

Many operations at the various national test ranges require the position of a test object to be determined as a function of time. The Air Force Global Positioning System (GPS) can provide this data. The test objects can vary from small devices being carried by a foot soldier to missiles or aircraft in flight. A considerable range exists in the velocities of the test objects and the rate at which data are required.

Test object position and velocity information is required both for use in performance analysis and to ensure that the vehicle does not stray outside the boundary of the test range. For range safety purposes, the data must be available in real time, usually from the instant of launch. In some cases relatively long periods of time prior to the beginning of the test are available for the GPS receiving equipment to lock on to signals from the satellite. In other cases, such as firing a missile from a tube, the signals from the satellite must be acquired very rapidly so that vehicle position can be determined.

GPS receivers currently available require long periods of time to acquire the signal from the satellites unless detailed vehicle position and velocity information is available at the time when signal acquisition is required. Acquisition time can run from several seconds to many minutes. This is unacceptable when the system is in use for range safety purposes or when recordings cannot be made to allow for a number of acquisition retries by means of multiple playbacks.

Acquisition time required by a conventional receiver is a function of two ingredients: (1) the knowledge of the frequency shift due to doppler effect of the signal to be tracked from the nominal frequency and (2) the range uncertainty between the satellite and the tracking system. It is necessary for a conventional receiver to search in both range and range rate (velocity). The range search must often be made through the 1023 chips of the GPS Clear Acquisition (C/A) code. Acquisition of the signal can only occur when the local replica of the code is within one chip of the received code and when the difference in frequency between the local oscillator signal and the received carrier is within the receiver frequency pull-in range. The pull-in range can vary from about 20 Hz to 500 Hz depending on the receivers' acquisition bandwidth. The reliability of acquiring this signal is dependent on the sweep rate in both range and frequency (range rate) and the signal strength of the received signal.

The fast acquisition receiver channel proposed herein can operate in a standard configuration, where the satellite signal is received by an antenna and fed directly into the receiver, or in a translator/transdigitizer mode where the signal is received by a translator or transdigitizer, shifted in frequency, and transmitted to the receiving site for further processing. In the case of the transdigitizer the signal would also be one bit quantized prior to transmission. The only difference between the operation of the fast acquisition receiver subsystem for these two methods is the amount of frequency (doppler) uncertainty of the signals to be processed.

Figure 1 is a block diagram of a typical system (satellites are directly tracked) using a fast acquisition channel. The system consists of a down converter, which receives the signal directly from the satellites at 1575.42 MHz and down converts this signal to baseband where it is 1 bit quantized at a high sample rate into I and Q components.

In the down conversion process the suppressed carrier of the signal, transmitted by the GPS satellites, is down converted to a frequency of 120 kHz. The I and Q components are required because the signal folds over, and if both are not

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used a 3 dB loss in signal to noise will result. The I and Q components are fed to the fast acquisition channel and to standard tracking channels. When the signals first become available the fast acquisition channel will acquire the signal from a chosen satellite. The time of the code epoch of the received signal and the frequency of the carrier will then be transferred to one of the standard tracking channels, which, with this data, can instantly acquire the signal. The fast acquisition channel then looks for the signal from the next satellite whose signal is to be acquired. This process continues until all tracking channels are locked. With reasonable signal levels, this process should be completed within five seconds.

The control and data collection system coordinates the operation of all the tracking channels and accepts the range and range rate data generated by the tracking channels, performs the necessary computation on this data, and provides the object position to the range control center. As an alternative, the measured range and pseudo-

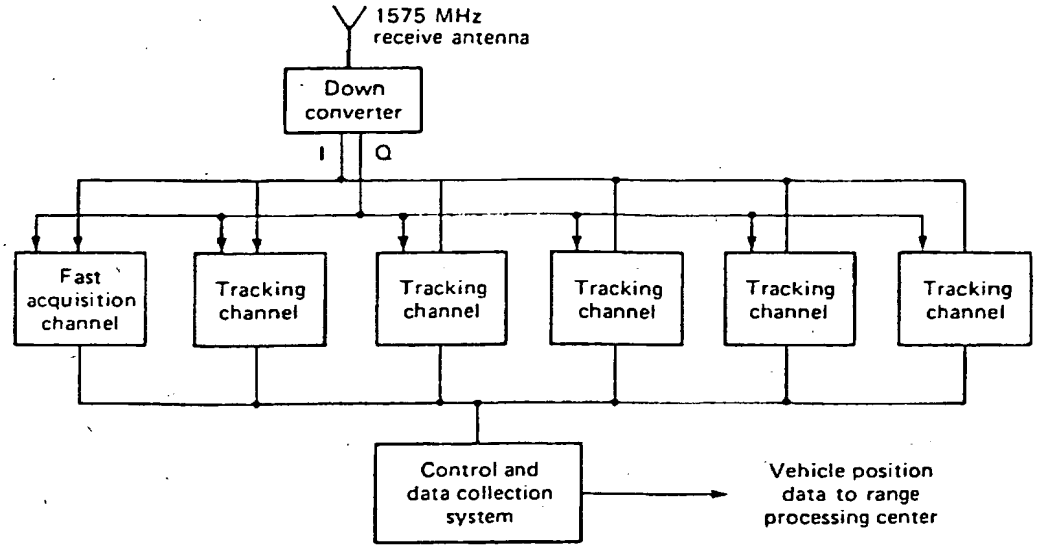

Fig. 1 Block diagram of receiver system.

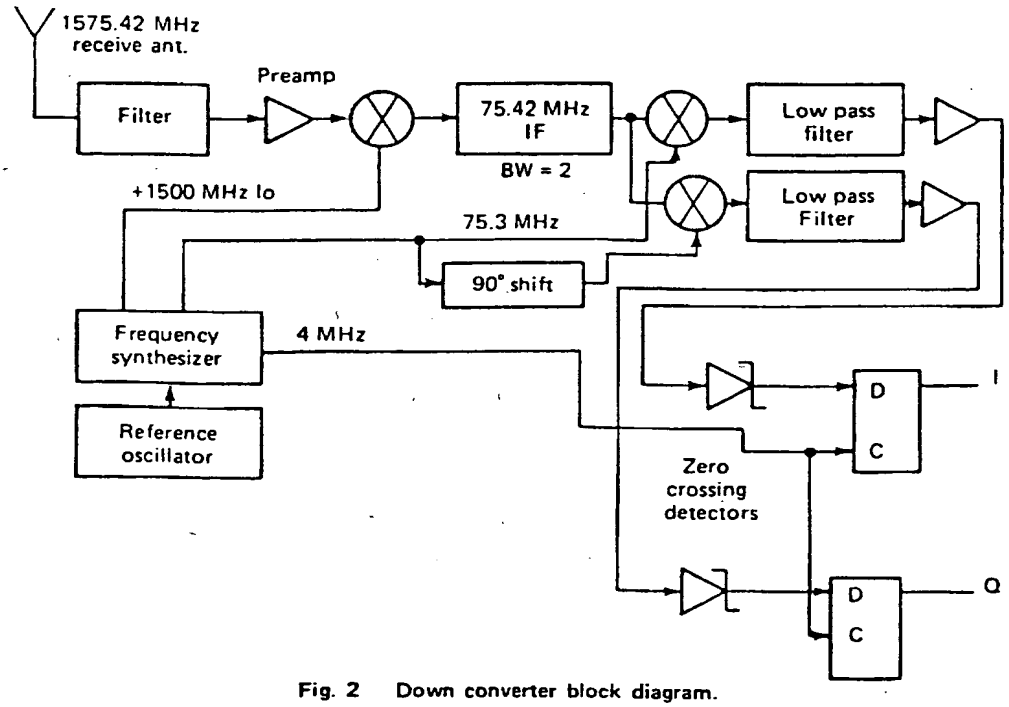

Fig. 2 Down converter block diagram.

ranges may be sent to the range processing center where the final vehicle position is computed.

Figure 2 is a block diagram detailing the down converter. The signal from the antenna is filtered and then amplified to establish the system noise figure. The signal is then down converted to a first IF frequency of 75.42 MHz, where it is further amplified. Then it is split into two components and down converted to a carrier frequency of 120 kHz. The local oscillator input to one of the mixers is shifted by 90 degrees to provide a quadrature output. The signals are then filtered by 1 MHz bandwidth lowpass filters and then are further amplified and applied to zero crossing detectors that provide a digital "1" level if the signal is positive and a digital "0" level if the signal is negative. These signals are then clocked by a pair of flip-flops whose clock frequency is at a nominal frequency of 1 MHz.

To aid in understanding how the fast acquisition receiver operates, let us examine how a standard digital tracking receiver, of the type developed at the Applied Physics Laboratory, operates. The fast acquisition receiver is a modified version of this type of receiver which is known as a WARNKE receiver and has been in operation at APL for the last five years. Figure 3 is a block diagram of this type of receiver. For simplicity only the I input signal channel is shown.

All logic in the receiver is digital in nature. Through use of software in the control processor, however, the receiver duplicates the operation of an analog type of receiver. Operation of the carrier tracking loop works in the following manner. The digitized input signal is applied to one input of an exclusive OR circuit. The signal to the other input is the CA code generated by a local code generator. The code rate is synthesized from the 5 MHz reference signal. The phase of the code can be varied by an electrically variable delay line. If the locally generated code exactly matches the code of the received signal the exclusive OR will remove the code leaving the signal carrier. This signal is fed into two other exclusive OR circuits. The second input of these circuits is from a local numerically controlled oscillator that generates a replica of the carrier. The input to the two exclusive OR's is 90 degrees out of phase. The output of these two circuits is fed to two up-down counters. These signals control whether the counters count up or down. The counting rate is typically at a 20 MHz rate.

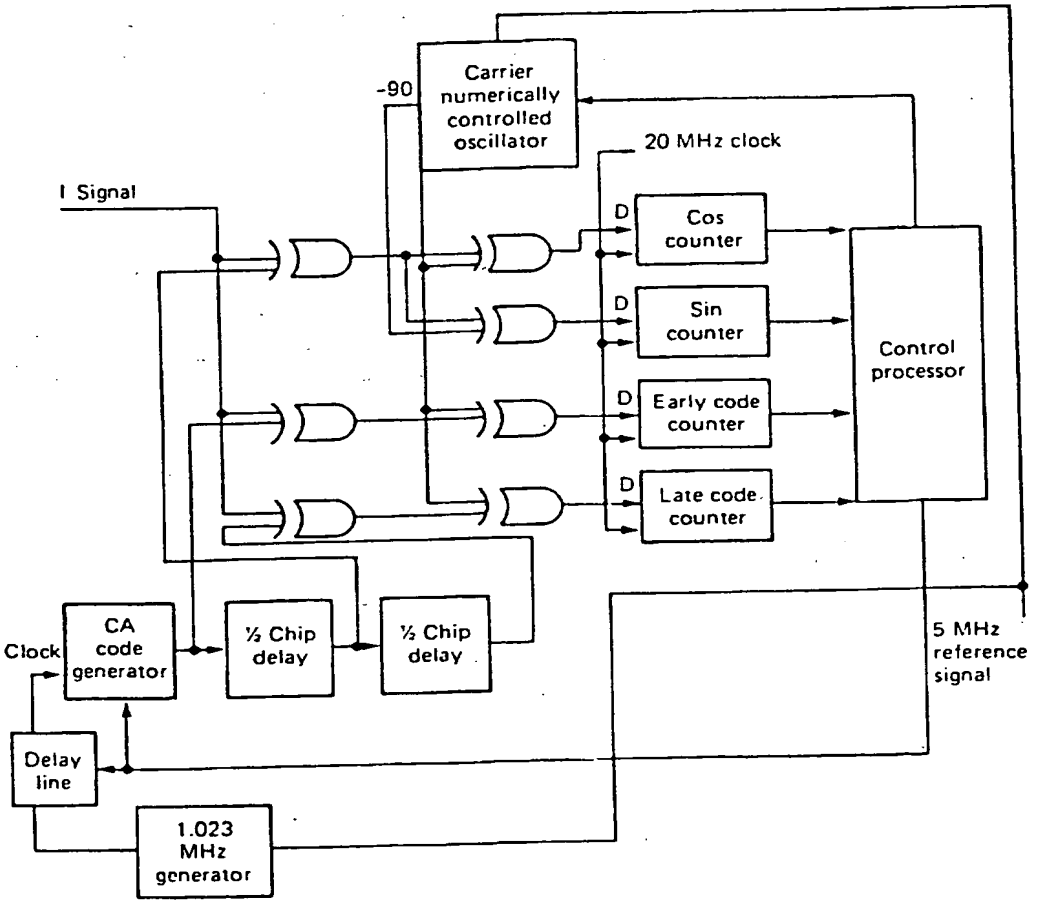

Fig. 3 Block diagram of digital tracking receiver.

The control processor is programmed so that every millisecond the contents of the two counters are read and then reset in such a way that no counts are lost. The processor computes a running sum of the counts from each counter over a period of 5 ms. If no signals are present the sums will be near zero. If a signal is present then at least one of the sums will be significantly different than zero. The value of the count is a function of the received signal level, the frequency error of the numerically controlled oscillator, and several other factors. A Costas loop operation is established where the sign of the output of one of the counters (the cosine counter) controls an inversion of the output of the other (sine) counter. Following this correction an arctangent is taken of the ratio of the two counts. This signal is indicative of the phase error and is independent of the amplitude of the received signal. This information is then used via a suitable transfer function to correct the frequency and phase of the numerically controlled oscillator to establish a phase lock condition.

The carrier can be tracked, however, only if the local code epoch is aligned with the code of the received signal. Initial lock is obtained by shifting the code while the carrier channels look for a correlation. Once an indication of a signal is present the early and late code counters are used to determine the error in code alignment. This is accomplished by feeding the two lower left exclusive OR circuits with code replicas that differ by one chip. If the received code is half way between these two codes then the output of the early code counter and the late code counter, once carrier lock is established, will be equal. If the received code is early with respect to the local code, the output of the early code counter will be high and that of the late code counter will be low.

The system has been implemented so that a tracking algorithm within the software, using the difference between the early and late correlator count, will correct the phase of the local code, establishing code phase lock. In practice, a second order (or higher) loop is established which causes the delay to change at a constant rate in order to maintain synchronization between the local code and the received code.

Figure 4 is a block diagram of the fast acquisition receiver. This receiver mimics the operation of the WARNKE receiver for detecting the presence of a signal. This receiver, however, because of the way in which it has been implemented, appears to be equal to 1023 receivers of the previously described type. This receiver has no advantage over the WARNKE type of receiver in that the frequency of the carrier numerical oscillator must be within 500 Hz of the frequency of the received signal. The advantage of this receiver is that a code search is not required because all possible code phases are simultaneously checked.

The heart of the fast acquisition receiver is the 64 bit correlation integrated

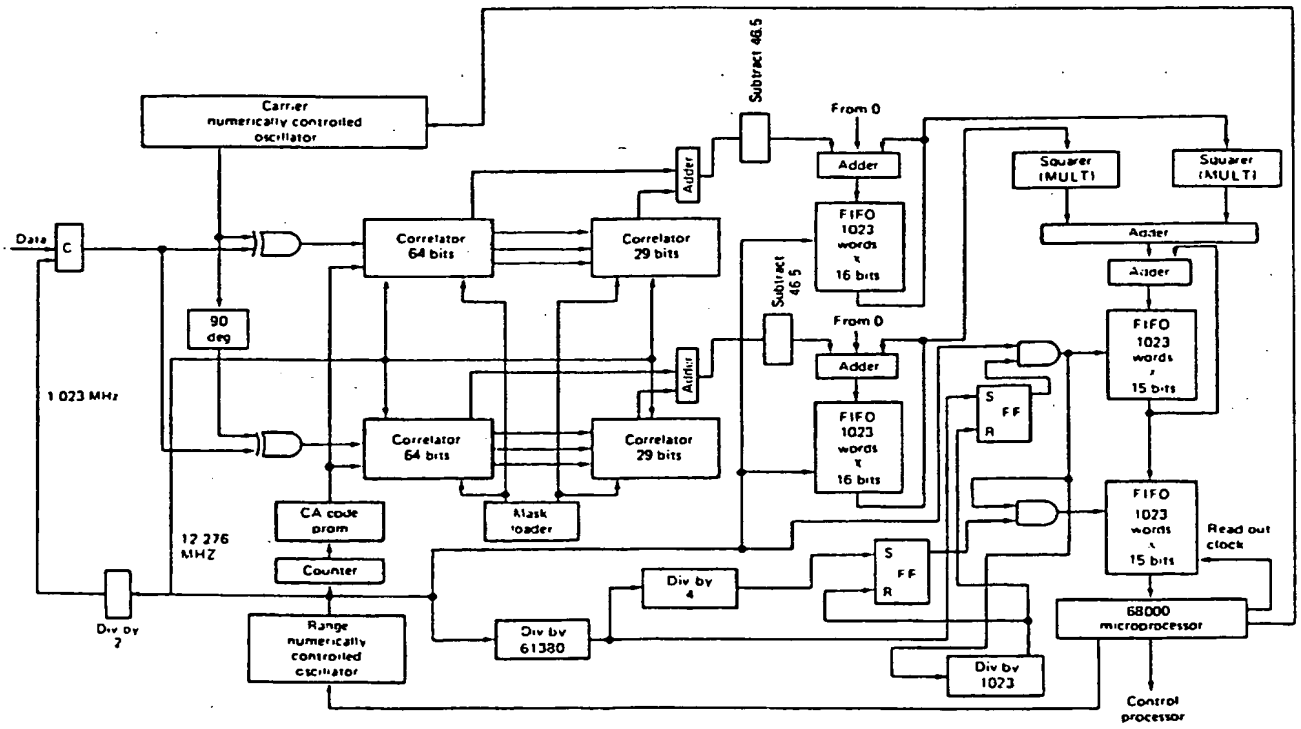

Fig. 4 Fast acquisition receiver block diagram.

circuits which are manufactured by the TRW Corporation. These circuits contain three 64-bit registers. One register is a mask register and determines how many bits within the chip will be involved in the correlation. All 64 bits will be used in the correlator chips (shown on the left edge of Figure 4) while only the first 29 bits are used in the other correlators. The other two registers hold the signal to be correlated and the reference pattern, which in this case is a portion of the 1023 bit gold code. A 7-bit output register provides a count of how many bits of the signal sequence match the reference sequence; if there is a perfect match an output of 64 would result. The two correlators in series provide a check on 93 bits simultaneously. The two outputs are added in a high speed adder to provide the total number of equal bits.

At the beginning of an integration period, the correlation value is placed into one position in a first in first out (FIFO) register that is 1024 (only 1023 used) words long. Following this operation the CA code replica in the correlator reference register is shifted right by 1 position. The correlation value for this position is then placed into the next position of the FIFO register. This process continues at 12 times the normal CA code rate of 1.023 MHz. On the twelfth shift of the code the data will also be shifted, but a correlation value will not be placed in the FIFO, because both the signal and code were concurrently shifted, and the correlation would be identical to the previous correlation. The process then continues.

After approximately 95.1 microseconds, or 93 steps of the incoming signal, 1023 correlation values will have been accumulated in the FIFO register. The shifting and correlation process continues, but from this point on the output of the FIFO is added to the correlation value to generate a correlation sum. At the end of 1 ms the 1023 gold code chips that are encoded within the received signal will have been correlated against 1023 different phases of the reference gold code. The results of these correlations will be stored in the FIFO. This process will continue for 4 ms, providing 5 ms of integration of the signal.

The process discussed above is accomplished for both sine and cosine phases of the numerically controlled oscillator signals by means of a double bank of correlators. In addition, a second set of four correlators will be used to provide a sampling rate of 2 megasamples per second instead of the 1 megasample per second rate that the system in Figure 4 would provide. The second set will minimize losses in the processing caused by a sampling rate at the Nyquist rate.

At the end of the 5 ms period, the output of the sine and cosine FIFO's are fed through multipliers to provide a squaring function, then fed through a pair of adders, and thence into another FIFO. The squaring operation is required to cancel out the effect of the message modulation on the signal. This is equivalent to squaring the carrier to remove the effects of the code. The 1023 words of data in the third FIFO are also recirculated and added to the input to provide additional integration. The number of additional cycles is currently planned at four. This will effectively provide 20 ms of integration which will result in an effective bandwidth of 50 Hz. Because of the presence of the squaring after each 5 ms of integration the circuit does have the ability to detect the presence of a signal over a reasonable frequency (doppler) range. It is currently estimated that signals in a total range of 500 Hz can be detected.

At the end of the 20 ms period the data will be shifted into the lower FIFO. The 1023 words of data will be transferred into the FIFO at 12.276 MHz. The data will then be shifted out into the processing computer at a much lower rate, depending on the computer software/hardware combination. The computer software will examine the 1023 words of data to determine if any of the values exceed a predetermined threshold, indicating the presence of a signal. The higher the value of the word the stronger the received signal. The computer would then transfer the epoch position, i.e., the number of the word with the highest count, and the current numerically controlled oscillator frequency data to the receiver assigned to track the signal. With this data the receiver should be able to rapidly acquire the signal.

Predicted Performance

The ability of the above described system to detect the presence of a signal is affected by a number of factors. Foremost is the level of the signal available and the gain of the associated receiving antenna. Related to this is the system integration time. The longer the integration time, the weaker the signal that can be detected. However, an increase in integration time reduces the frequency range (doppler) over which signals can be detected. This results in increased acquisition time.

The sensitivity of the system is also a function of the sampling rate, and if a full I and Q processing system is used. If an I only implementation is used a 3 dB loss in system sensitivity will result. If a 4 MHz sampling rate was used an improvement in sensitivity of 2 to 3 dB would occur. The complexity of the system would be doubled.

The system, as discussed above, using a 2 MHz sampling rate and both I and Q processing will provide an output signal-to-noise ratio of about 20 dB assuming a signal input of -130 dBm into a 4 dB front end. In most cases, the antenna gain will be significantly less than 0 dB, which will reduce the effective signal level and impact the final signal-to-noise ratio.

Development of the receiver is just beginning. The system will be breadboarded and tested extensively to evaluate system performance.